Data Base Information for ROC and TBM Chips After Wafer Testing

Cristian Gingu, Boris Baldin, Umesh Joshi
Fermi National Accelerator Laboratory, Batavia, IL 60510
- November 2005 -

Introduction

This document describes what information is stored in CMS (construction) data base after ROC and TBM wafer testing.

During the wafer test the test program is writing a number of XML files for each chip. After the test is finished, these files are (automatically) read by some load application (developed by data base group) and written into the data base according to the data base format. We'll not discuss here either the structure of XML files or details related to the file uploading and retrieving information from the data base. Instead we'll present here only what information is passed to the XML files (and thus to the data base) after chips on the wafer are tested. For further details of each test procedure refer to doc#467-v2 (for TBM05) and doc#329-v2 (for ROC).

1. XML files for TBM.

Up to date we have tested five TBM wafers. The test data is currently loaded into the data base. The test results are structured in three XML files (for each chip). For the next TBM wafers (expected in January 2006) we plan to increase the number of XML files and add more files to cover "GROUP4 - Analog Output" (see doc#467-v2 for details).

1.1. FailCode files.

These files have a name like W5_MBFR4GT_1_0_T99FailCode.xml. This name is an example for chip#0 in reticule#1 from wafer#5. The information passed to the data base is just one number (decimal value of the FailCode) as described in doc#467-v2. For easy reference, we show below the bit encoding described in that document. Note that Txx is a test number listed in the doc#467-v2.

Bit0= error on T11
Bit1= error on T12
Bit2= error on T13
Bit3= error on T14
Bit4= error on T51
Bit5= error on T52

Bit6= error on T61
Bit7= error on T62
Bit8= reserved
Bit9= reserved
Bit10= reserved
Bit11= reserved
Bit12= error on T67
Bit13= error on T68
Bit14= error on T69
Bit15= error on T70
Bit16= error on T71
Bit17= error on T72
Bit18= error on T73
Bit19= error on T20 or T21 or T22 or T23 or T24
Bit20= error on T25 or T26
Bit21= error on T27 or T28
Bit22= error on T29
Bit23= error on T31 or T32 or T33 or T34
Bit24= error on T35 or T36
Bit25= error on T41 or T42 or T43
Bit26= error on T44 or T45 or T46 or T47
Bit27= error on T48 or T49

For example, if the FailCode number is zero, the TBM chip passed all the tests, and if it is 16 that means the TBM chip failed on T51 test.

For easy reference we show below the name of each test.

GROUP 1. Hub and Ports

T11PowerSupply
T12Registers
T13ROCPorts
T14HubAddress

GROUP 2. TBM Triggers

T20CalibModeCSRTrig
T21SyncModeNormTrigg
T22SyncModeCSRTrigg
T23ClearEventCounterModeNormTrigg
T24ClearEventCounterModeCSRNormTrigg
T25ClearEventCounterModeROCResetTrigg
T26ClearEventCounterModeNormTrigg
T27ClearEventCounterModeTBMResetTrigg
T28ClearEventCounterModeNormTrigg
T29ReadoutMode20MHz

GROUP 3. Stack

T31TBMStack32NormTrigg
T32TBMStack32StackCount
T33TBMStack32StackEvent
T34TBMStack32ReadVerify
T35TBMStack24NormTrigg
T36TBMStack24ReadVerify

GROUP 4. Analog Output

T41ScanRegAnaInpBias
T42ScanRegAnaOutBias
T43ScanRegAnaOutGain
T44RiseFallTimesP0
T45RiseFallTimesP1
T46RiseFallTimesP2
T47RiseFallTimesP3
T48PulseLinP0
T49PulseLinP2

GROUP 5. Single TBM

T51SingleTBMA
T51SingleTBMAOnly
T52SingleTBMB
T52SingleTBMBOnly

GROUP 6. Miscellaneous

T61IgnoreIncommTrigg
T62DisableTrigg
T67InjectROCResetTriggTBMA
T68InjectROCResetTriggTBMB
T69InjectCalibTriggTBMA
T70InjectCalibTriggTBMB
T71InjectTBMResetTriggTBMA
T72InjectTBMResetTriggTBMB
T73ClearStackCounter

We agreed that the data base GUI interface application will provide a decoded value of the FailCode number.

1.2. PowerSupply files.

These files have a name like W5_MBFR4GT_1_0_T11PowerSupplyTBM.xml. The information passed to data base should be obvious from the following example.

<VDIG>2.486</VDIG> - Digital Supply Output in Volts
<VANA>2.474</VANA> - Analog Supply Output in Volts
<VCAPVD>2.092</VCAPVD> - Decoupling capacitor voltage in Volts
<VCAPVA>2.053</VCAPVA> - Decoupling capacitor voltage in Volts
<VCAPLVDSLOW>1.027</VCAPLVDSLOW> - Decoupling capacitor voltage in Volts
<VCAPLVDSHIGH>1.237</VCAPLVDSHIGH> - Decoupling capacitor voltage in Volts
<IDIG>9.85</IDIG> - Digital Supply Current in mA
<IANA>19.97</IANA> - Analog Supply Current in mA
<POWERSUPPLY_ERRCODE>0</POWERSUPPLY_ERRCODE>

For <POWERSUPPLY_ERRCODE> details refer to doc#467-v2.

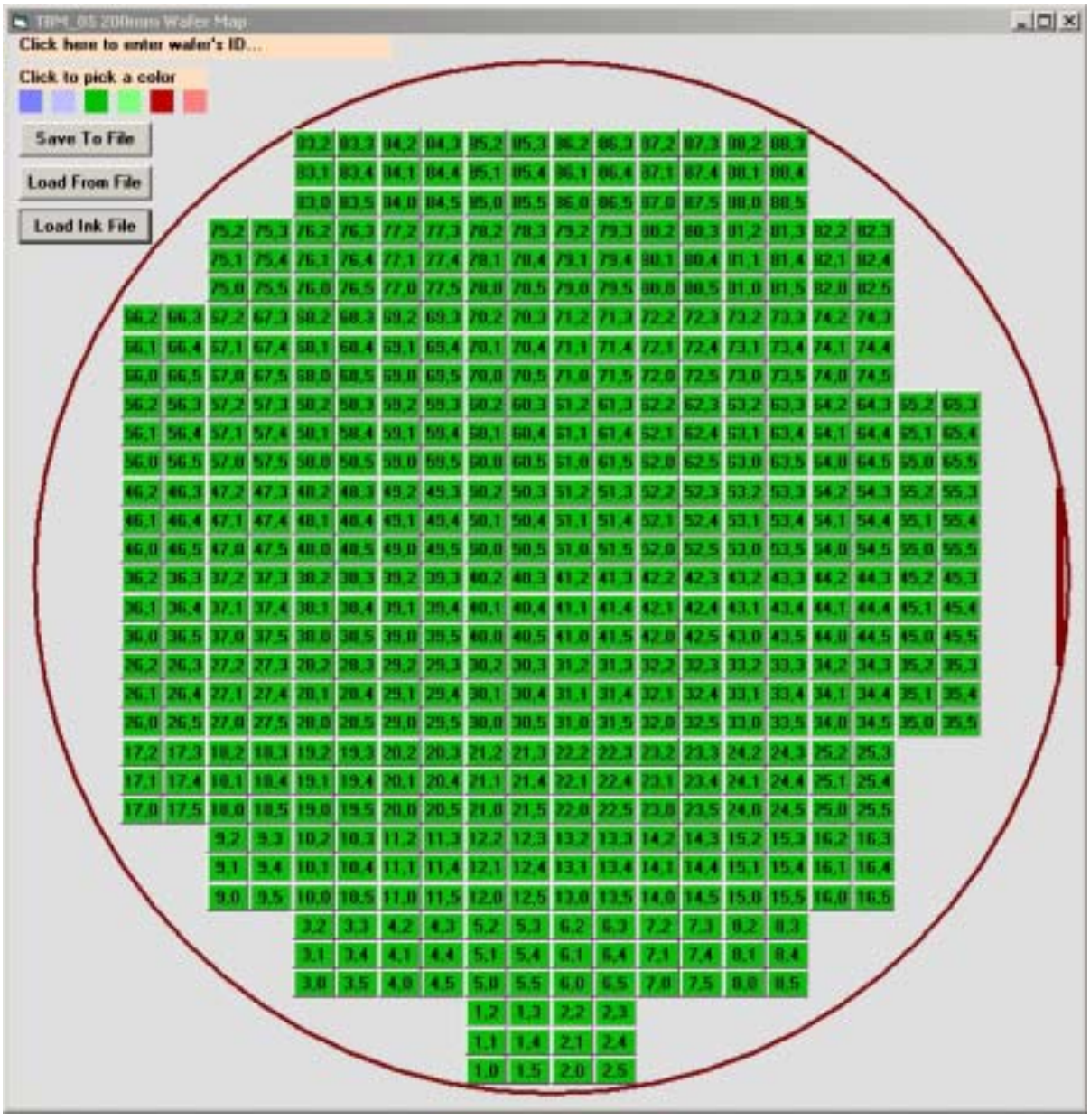
1.3. AnalogLevelsStat files.

These files have a name like W5_MBFR4GT_1_0_T34XAnalogLevelsStat.xml. The information passed to the data base should be obvious from the example below. Please note that these are ADC counts readout values while doing T34TBMStack32ReadVerify test. This data IS NOT reflected in any way in the FailCode. What it shows is basically the offset and gain variation of TBM chip. Currently, we have agreed to limit baseline and UB level variations to +/- 200 ADC counts (which is about ±20% of the average UB value). The chips outside these limits will be labeled failed on test T34.

<STAT_TBMA_BLMIN>2146</STAT_TBMA_BLMIN>
<STAT_TBMA_BLMAX>2192</STAT_TBMA_BLMAX>
<STAT_TBMA_BLAVG>2167</STAT_TBMA_BLAVG>
<STAT_TBMA_UBMIN>890</STAT_TBMA_UBMIN>
<STAT_TBMA_UBMAX>946</STAT_TBMA_UBMAX>
<STAT_TBMA_UBAVG>916</STAT_TBMA_UBAVG>
<STAT_TBMA_L0MIN>2126</STAT_TBMA_L0MIN>
<STAT_TBMA_L0MAX>2162</STAT_TBMA_L0MAX>
<STAT_TBMA_L0AVG>2143</STAT_TBMA_L0AVG>
<STAT_TBMB_BLMIN>2060</STAT_TBMB_BLMIN>
<STAT_TBMB_BLMAX>2094</STAT_TBMB_BLMAX>
<STAT_TBMB_BLAVG>2078</STAT_TBMB_BLAVG>
<STAT_TBMB_UBMIN>741</STAT_TBMB_UBMIN>
<STAT_TBMB_UBMAX>785</STAT_TBMB_UBMAX>
<STAT_TBMB_UBAVG>758</STAT_TBMB_UBAVG>
<STAT_TBMB_L0MIN>2036</STAT_TBMB_L0MIN>
<STAT_TBMB_L0MAX>2066</STAT_TBMB_L0MAX>
<STAT_TBMB_L0AVG>2051</STAT_TBMB_L0AVG>

2. Wafer map for TBM.

The wafer map below shows the numbering scheme used for labeling TBM chips. There are 88 reticules and each reticule consists of 6 TBM chips shown in this wafer map and also some other chips not shown here.



3. ROC XML files.

As of today, there is not yet any test data loaded into the data base for the ROC. But we have constructed the XML files and we are waiting for confirmation from the data base group to provide real test data. Currently, for each chip there are ten XML files that we intend to use for the data base.

3.1. InitSettings files.

These files have a name like W5_XM4F4ZT_30_3_InitSettings.xml and the info passed to data base contains the initial settings for both ROC chip and PSI46 Interface Board.

3.2. FailCode files.

The "FailCode" XML file contains basically two types of information:

a) The "FailCode" decimal number.
b) The number of failed pixels in each column.

The following example should illustrate this.

```
<FAIL_CODE>26672</FAIL_CODE>
<FAIL_PIX_COL_1>0</FAIL_PIX_COL_1>
<FAIL_PIX_COL_2>0</FAIL_PIX_COL_2>
<FAIL_PIX_COL_3>0</FAIL_PIX_COL_3>
<FAIL_PIX_COL_4>0</FAIL_PIX_COL_4>
<FAIL_PIX_COL_5>0</FAIL_PIX_COL_5>
……
<FAIL_PIX_COL_40>0</FAIL_PIX_COL_40>
<FAIL_PIX_COL_41>1</FAIL_PIX_COL_41>
<FAIL_PIX_COL_42>3</FAIL_PIX_COL_42>
<FAIL_PIX_COL_43>0</FAIL_PIX_COL_43>
….
<FAIL_PIX_COL_51>0</FAIL_PIX_COL_51>
<FAIL_PIX_COL_52>0</FAIL_PIX_COL_52>
```

The "FailCode" number (see also doc#329-v2) is encoded as following:

Bit 0 is set when digital supply current is too low.
Bit 1 is set when digital supply current is too high.
Bit 2 is set when analog supply current is too low.
Bit 3 is set when digital supply current is too high.
Bit 4 is set when DAC Linearity Test negative deviation is too low.
Bit 5 is set when DAC Linearity Test positive deviation is too high.
Bit 6 is set when DAC Linearity Test found a response length error.

Bit 7 is set when DAC Linearity Test found a FIFO full flag error.
Bit 8 is set when Token Out Test failed.
Bit 9 is set when I2C Test failed.
Bit 10 is set when I-V Curve failed.
Bit 11 is set when Time Stamp Buffer Test failed.
Bit 12 is set when Data Buffer Test failed.
Bit 13 is set when WBC Register Test failed.
Bit 14 is set when 1-5 pixels failed.
Bit 15 is set when 6-10 pixels failed.
Bit 16 is set when 11-20 pixels failed.
Bit 17 is set when >20 pixels failed.

3.3. PowerSupply files.

These files have a name like W5_XM4F4ZT_30_3_PowerSupply.xml and the info passed to the data base contains all currents (mA) and voltages (Volts) as measured before and after chip setup.

3.4. I2C files.

These files have a name like W5_XM4F4ZT_30_3_I2C.xml and the info passed to data base contains the results of I2C test as described in doc#329-v2.

3.5. IVANA_CURVE files.

These files have a name like W5_W5_XM4F4ZT_30_3_IVANA_CURVE.xml and the info passed to the data base contains the Iana current (mA) as a function of Vana setting (decimal) while we search for the optimum Vana setting at which Iana=24mA.

The following example should illustrate this.

<DATA><VANA_DAC>32</VANA_DAC><IANA>1.78</IANA></DATA>
<DATA><VANA_DAC>64</VANA_DAC><IANA>4.91</IANA></DATA>
<DATA><VANA_DAC>96</VANA_DAC><IANA>12.03</IANA></DATA>
<DATA><VANA_DAC>128</VANA_DAC><IANA>25.28</IANA></DATA>
<DATA><VANA_DAC>160</VANA_DAC><IANA>43.94</IANA></DATA>
<DATA><VANA_DAC>192</VANA_DAC><IANA>58.80</IANA></DATA>
<DATA><VANA_DAC>112</VANA_DAC><IANA>18.21</IANA></DATA>
<DATA><VANA_DAC>120</VANA_DAC><IANA>21.20</IANA></DATA>
<DATA><VANA_DAC>124</VANA_DAC><IANA>23.17</IANA></DATA>
<DATA><VANA_DAC>126</VANA_DAC><IANA>24.29</IANA></DATA>
<DATA><VANA_DAC>125</VANA_DAC><IANA>23.63</IANA></DATA>

3.6. DAC_RESPONSE_CURVE files.

These files have a name like W5_XM4F4ZT_30_3_DAC_RESPONSE_CURVE.xml and the info passed to data base contains the DAC linearity test as described in doc#329-v2.

3.7. DataBuffer files.

These files have a name like W5_XM4F4ZT_30_3_DataBuffer.xml and the info passed to data base contains the Data Buffer test results as described in doc#329-v2.

NOTE: Although this test result (PASS or FAIL) is reflected in bit12 of FailCode number, we may want to keep also detailed test results for (eventually) PSI failure type comparison. Also, the data base table associated with it is already verified by data base group.

3.8. TimeStampBuffer files.

These files have a name like W5_XM4F4ZT_30_3_TimeStampBuffer.xml and the info passed to data base contains the Time Stamp Buffer test results as described in doc#329-v2.

NOTE: Although this test result (PASS or FAIL) is reflected in bit11 of FailCode number, we may want to keep also detailed test results for (eventually) PSI failure type comparison. Remember that this is the only test that we do at 5MHz because of the ROC limitations of the calibration pulser circuitry. The data base table associated with it is already verified by data base group.

3.9. ROCHistograms files.

These files have a name like W5_XM4F4ZT_30_3_ROCHistograms.xml and the info passed to the data base will allows the data base user to generate a histogram plot of the following parameters:

a) Row and Column address analog levels.
b) Charge readout.
c) Analog value of Base Line signal.
d) Analog value of Ultra Black signal.
e) Analog value of Black signal.
f) Vcal register settings at which pixel fired.

These histograms are constructed from all 4160 pixel responses. The bin width of the histogram is 16 ADC counts. This value allows a fairly good separation of Row and Column address levels, typically 1 to 4 bins. The total number of bins is 256.

3.10. PixelCodeErrors files.

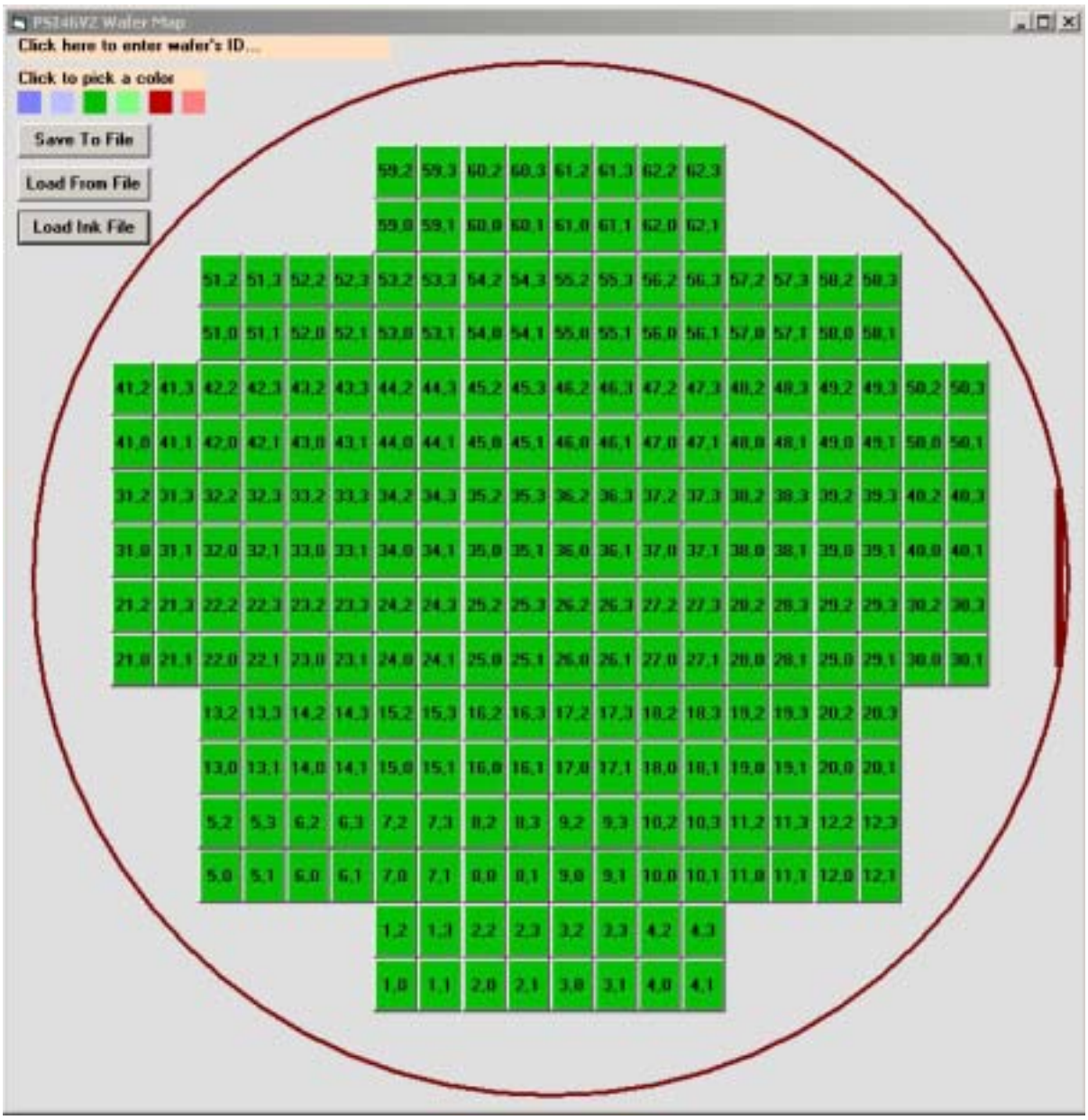
These files have a name like W5_XM4F4ZT_30_3_PixelCodeErrors.xml and the info passed to the data base represents a string character for each pixel. If the string is null, the pixel passed all tests. If the pixel failed some tests, then the string encodes the failure type. Description of pixel failure codes can be found in the ROC test reports.

The following example illustrates two pixels not responding, in Column=37, Row=1 and Row=2.

<COL>36</COL><ROW>80</ROW><ERR></ERR>
<COL>37</COL><ROW>1</ROW><ERR>N2,N3,<ERR>
<COL>37</COL><ROW>2</ROW><ERR>N1,N2,N3,<ERR>
<COL>37</COL><ROW>3</ROW><ERR><ERR>

4. Wafer map for ROC.

The wafer map below shows the numbering scheme used for labeling ROC chips. There are 62 reticules and each reticule consists of 4 ROC chips shown in this wafer map.



Conclusions

The proposed formats of the data for wafer testing are intended as a first approach to creating production version set of parameters for the TBM and ROC chips. Further improvements will be implemented when necessary.